Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A circuit for generating an internal clock signal, comprising:

an operating frequency decision unit for determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency and outputting an detecting signal; [[and]]

an internal clock signal generator for ~~waveform-shaping the external clock signal and~~ generating an internal clock signal ~~depending on the detecting signal of the operating frequency decision unit, or generating~~ or outputting the external clock signal as the internal clock signal ~~as it is~~, the internal clock signal generator comprising:

a delay unit for delaying the external clock signal by some time; and

a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is.

2. (Previously Presented) The circuit as claimed in claim 1, wherein the operating frequency decision unit comprises an inverter for inverting a level of a most significant bit of the CAS latency.

3. (Previously Presented) The circuit as claimed in claim 1, wherein the CAS latency has a value of 0 to 7 and the operating frequency decision unit generates the detecting signal if the value of the CAS latency is over 4.

4. (Previously Presented) The circuit as claimed in claim 1, further comprising a mode register for storing the CAS latency.

5. (Currently Amended) The circuit as claimed in claim 1, wherein ~~the internal clock signal generator~~ the pulse-shaping unit comprises:

~~a delay unit for delaying the external clock signal by some time; and~~

~~a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is~~

a first NAND gate for logically combining the external clock signal with the output signal of the delay unit depending on the detecting signal of the operating frequency decision unit;

a second NAND gate into which the external clock signal and the output signal of the first NAND gate are inputted; and

an inverter for inverting the output signal of the second NAND gate.

6. (Canceled)

7. (Previously Presented) A circuit for generating an internal clock signal, comprising:

an operating frequency decision unit for determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency and outputting an detecting signal;

an internal clock signal generator for waveform-shaping the external clock signal and generating an internal clock signal depending on the detecting signal of the operating frequency decision unit, or generating the external clock signal as the internal clock signal as it is, the internal clock signal generator comprising:

a delay unit for delaying the external clock signal by some time; and

a pulse-shaping unit for logically combining the external clock signal with the output of the delay unit and generating the internal clock signal depending on the output detecting signal of the operating frequency decision unit, or generating the external clock signal as the

internal clock signal as it is, the pulse-shaping unit comprising a first NAND gate for logically combining the external clock signal with the output signal of the delay unit depending on the detecting signal of the operating frequency decision unit, a second NAND gate into which the external clock signal and the output signal of the first NAND gate are inputted, and an inverter for inverting the output signal of the second NAND gate.

8. (Currently Amended) The circuit as claimed in claim [[5]]1, wherein the delay unit includes a RC delay circuit.

9. (Original) The circuit as claimed in claim 8, wherein the delay unit comprises:

a first inverter for inverting the external clock signal; a number of resistors serially connected between the output of the first inverter and a first node;

a number of MOS capacitors connected between the first node and a ground; and

a second inverter connected between the first node and an output terminal.

10. (Previously Presented) The circuit as claimed in claim 9, wherein the delay unit further comprises:

first fuses connected in parallel to the resistors, respectively, and can be blown; and

second fuses connected in parallel to the MOS capacitors, respectively, and can be blown.

11. (Currently Amended) The circuit as claimed in claim [[5]]1, wherein the delay unit comprises:

a first inverter for inverting the external clock signal; a number of resistors serially connected between the output of the first inverter and a first node;

a number of MOS capacitors connected between the first node and a ground; and

a second inverter connected between the first node and an output terminal.

12. (Previously Presented) The circuit as claimed in claim 11, wherein the delay unit further comprises:

first fuses connected in parallel to the resistors, respectively, and can be blown; and

second fuses connected in parallel to the MOS capacitors, respectively, and can be blown.

13. (Original) The circuit as claimed in claim 1, wherein the internal clock signal has the same pulse width as that of the external clock signal or has the pulse width corresponding to delay time of the delay unit.

14. (Currently Amended) A method of generating an internal clock signal, comprising the steps of:

determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency; and

waveform-shaping the external clock signal and generating an internal clock signal if the external clock signal is the low frequency ~~depending on a result of the determination step, or generating the external clock signal~~, or outputting the internal clock signal having the same pulse width and the same frequency as the external clock signal if the external clock signal is the high frequency ~~as the internal clock signal as it is~~, depending on a result of the determination step.

15. (Canceled)

16. (Previously Presented) A method of generating an internal clock signal, comprising the steps of:

determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency; and

waveform-shaping the external clock signal and generating an internal clock signal depending on a result of the determination step, or generating the external clock signal as the internal clock signal as it is,

wherein the CAS latency has a value of 0 to 7 and the external clock signal is determined as the high frequency if the value of the CAS latency is over 4.

17. (Currently Amended) A method of generating an internal clock signal, comprising the steps of:

determining whether an external clock signal is a low frequency or a high frequency depending on a column address strobe (CAS) latency; [[and]]

generating a delayed external clock signal by delaying the external clock signal by some time; and

waveform-shaping the external clock signal using the delayed external clock signal and generating an internal clock signal depending on a result of the determination step, or generating the external clock signal as the internal clock signal as it is,

wherein the step of generating the clock comprises the steps of:

waveform-shaping the external clock signal by logically combining the external clock signal with the delayed external clock signal and generating the internal clock signal if the external clock signal is the low frequency; and

generating the external clock signal as the internal clock signal as it is if the external clock signal is the high frequency.

18. (Currently Amended) A circuit for generating an internal clock signal, comprising:

an operating frequency decision unit for outputting a detecting signal which indicates whether an external clock signal is a low frequency or a high frequency in response to a column address strobe (CAS) latency; and

an internal clock signal generator for generating an internal clock signal by waveform-shaping the external clock signal, or for outputting the external clock signal ~~as it is for using the external clock signal~~ as the internal clock signal so that the internal clock signal has the same pulse width and the same frequency as the external clock signal, in response to the detecting signal.

19. (Previously Presented) The circuit as claimed in claim 18, wherein the operating frequency decision unit comprises an inverter for inverting a level of a most significant bit of the CAS latency.

20. (Previously Presented) The circuit as claimed in claim 18, wherein the internal clock signal generator comprises:

a delay unit for delaying the external clock signal by some time;

a first NAND gate for logically combining the external clock signal with the output signal of the delay unit depending on the detecting signal of the operating frequency decision unit;

a second NAND gate into which the external clock signal and the output signal of the first NAND gate are inputted; and

an inverter for inverting the output signal of the second NAND gate.